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Design of I2C Protocol

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ABSTRACT: Inter Integrated Circuit, abbreviated as I2C, was developed by Philips Semiconductor approx. 20 years ago by a serial bus short distance protocol to facilitate connectivity between the core on the board and various other core ICs. This implementation note is intended to explain how I2C is distinct from other serial buses, and to explain the characteristics of different serial buses. In this implementation note, the features and operation of I2C as well as example code illustrated how I2C is implemented will also be illustrated. The I2C (Inter IC) protocol is a basic two-line protocol used for data sharing between computers. I2C is simple, half duplex protocol bidirectional. Philips Semiconductor (NXP Semiconductors) has developed this serial Communication Protocol. It is now used by almost all leading IC manufacturers.

KEYWORDS: Master, Slave, SDA, SCL, Verilog HDL.

I.INTRODUCTION

The overall definition of connectivity through serial buses SPI, UART, I2C, CAN, USB, IEE1394 and so on are the most common serial bus connectivity protocols on the market today. Inter-integrated Circuit stands for I2C. In order to ensure seamless connectivity between integrated circuits (ICs) from different manufacturers, Phillips Electronics created the I2-C bus protocol. Microcontrollers, LCDs, memory appliances, PCs, mobile phones, TV, ADCs, DACs and other applications can be used in systems with an I2 C bus. It's I2C (Inter-Integrated Circuit, I-squared-C, I-two-C or IIC[1]) and I2-c is a serial line clock (SCL) line, as well as a serial line (SDA), which has two bidirectional signals in the I2 C bus. Every bus-connected device has a unique address to identify the communications device. The protocol shall contain a variety of requirements. The I2C between devices inside a TV set was initially developed by Philips. For eg, embedded systems include simple I2C compliant devices such as EEPROMs, thermal capable sensors and real-time clocks. I2C is also used as a signal management interface with different device interfaces for the programme. Hundreds of I2 C-compatible systems are supplied in Philips, Xicor, Siemens and other suppliers. Usually, I2C buses can be faster than 400 kbps. There are several protocols that send and receive data from one device to another. But I2c is the simplest protocol because it only has two wire lines SDA (Serial Data Line) and SCL (Serial Clock line) and it has the power of a multi-master unlike the SPI (Serial Peripheral Interface).I2C is a sync protocol, unlike UART.

In this paper, it proposes The I2C is a synchronous protocol, which makes it possible for a master computer to begin contact with a slave device. 2.2 SCL, SDA Lines Mechanically, the I2C bus consists of two active wires. Active cables, such as SDA and SCL. SDA is a two-way signal, SCL a one-way signal. SDA is a "Serial" DA's Line SCL "serial" Clocks I 2 C "serial interface that uses only the 2 signals below to interchange data with another system on a standard basis. SDA-Data sent from one computer to another was sent in this line. SCL – The master computer is generated and controls the sending and reading of data. 2.3 Data Transmission 8 bits of information are passed to the data block. Data are transmitted over the SDA line and SCL generates a clock. You should align the clock to show that each bit is a "1" or a "0." SDA data is accurate only if SCL is large. If SCL is not big, the data could beA control code, an address or data may be 8 bits of data. We will link a serial EEPROM (24C02) to the bus in this presentation and analyse the signals. Related signals which not be equivalent with other I2C equipment. The state of ACK and NACK. A system can 'ACK' or accept a byte switch by lowering the SDA line on the 9th clock of SCL pulse. It's the 9 bits of a switch – 8 bits are clocked on the data, and the 9th bit is ringed on the object getting data. The unit signs a "ACK" if it pushes this bit low. Alternatively, the SDA line is permitted to float high so "NACK" is not remembered. 2.4 Master and Slave — Master or slave modules are on the I2C bus. A slave cannot start transmitting via the I2C bus, only a master will. · At the I2C bus there may normally be several slaves, but normally only a master remains. The owner as well as the slave will pass.

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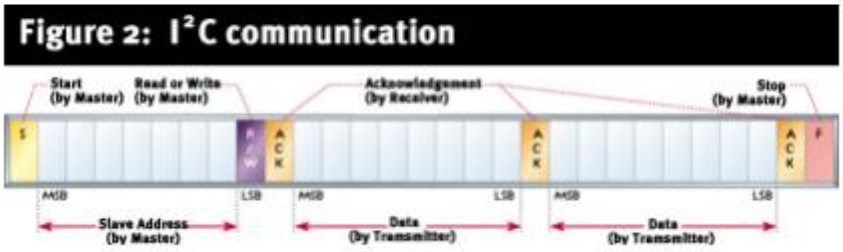
II. DESIGN METHODOLOGY

I 2 C is designed for devices interfacing on one board and can be positioned within a closed structure through several boards. One example is a host CPU that interacts with user interface devices placed on a different front panel board using I2C. As seen in Figure 1, I2C is a two-wire serial bus. Chip selection or arbitration logic is not required, making it inexpensive and convenient to implement in hardware. The serial and serial clocks of the two I2C signals are. Together, these signals allow 8-bit byte serial transmission of data 7-bit system addresses and two-wire serial bus bits. In the middle of a trade, an I2C slaves will keep the master with what is called a clock stretch (slave holds down SCL until it is ready). Moreover, several masters can be supported in the I2C protocol. One or two slaves may be on the bus. Masters and slaves will receive and send bytes of data. The hardware slave computer compatible with I2C has a predefined device address which can be programmed in the lower bits of the monitor. At the beginning of each exchange, the master transmits the device address of the intended slave. Each slave has to watch the bus and respond only to his / her own mail. This address scheme restricts the number of slave devices which are equivalent to the number of user-configurable address bits which may occur on the unconstrained I2C bus.



The I2C signalling protocol includes an addressing unit, a read / writes flag and a fast acceptance process. The general (broadcast) and 10-bit expanded addressing are other components of the I2C protocol. Standard I2C systems run with up to 100Kbps and fast-mode models with up to 400Kbps. The CPU or microcontroller on the machine is normally the I2 C master. Also hardware for the I2C protocol is included in certain microcontroller. An all-software implementation can also be designed with a pair of I / O pins for general purposes. The bus protocol does not place any in-time limits in the CP U outside the application, because the I2C master monitors the transaction time. The high and low logics for a set I2C are defined at 3.0 V/1.5 V, which is defined at 0.7*Vdd and 0.3*Vdd for dependent I2C respectively. Usually, the I2C pull-up resistor values are 1k to 3.0V Vdd and 1.6k to 5VV Vdd. Operating temperatures are usually between -40 ° C

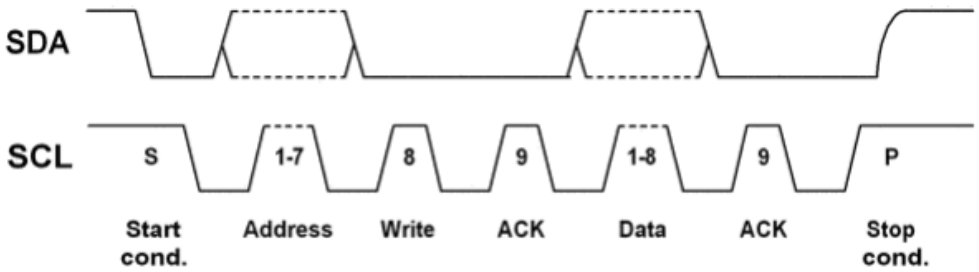


Figure 3: I2C addressing

III. I2C COMMUNICATION PROTOCOL

In this scheme, Master gives the slave address he needs to write to or read from. There are several modes for addressing this problem, such as a 7 bit, 10 bit and a free data addressing mode, but in this project we have a 7 bit mode addressing mode. We have a 7 bit mode slave address transmitted bit by bit over the SDA side. When reading / writing is 0, then

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the master will write to the slave computer. When read / write bit is one, the master will read from the slave device. Any transformation takes place on SDA, with a low SCL. Although SCL is high, the data needs to be stable.Data Transfer: If the slave address fits the master address, the slave sends ACK to the master. Once the slave receives an acknowledgment, the data is transmitted bit by bit by SDA by the master to the slave(if the reading / pressure bit is zero) or to the slave to master (if the read / press bit is one), depending on the read / pass write bit. − OUT STOP: After receiving ACK or NACK (during the writing process), the transition from low to high SDA is finished by last byte master. If master wants to send again the same slave, master will send REPEATED START condition instead of STOP. When reading, master transmits NACK after last data byte and then stops transmission.

IV. I2C BENEFITS

Well-known bus has been a global standard for 20 years.
• Stanadrd, which has been embraced by sectors such as Network, Consumer and Automotive.
· Used in many applications, such as mobile phones, PDAs, DVDs and installation boxes.
• Serial interface with two wire.
• Designed for many years to remain on the market and Usage of giants such as HP, Compaq, IBM, Cisco, Intel, Nokia and so forth.

V. RESULT AND DISCUSSION

In the fig 1, it shows the Simulation Results of the corresponding I2C communication protocol.

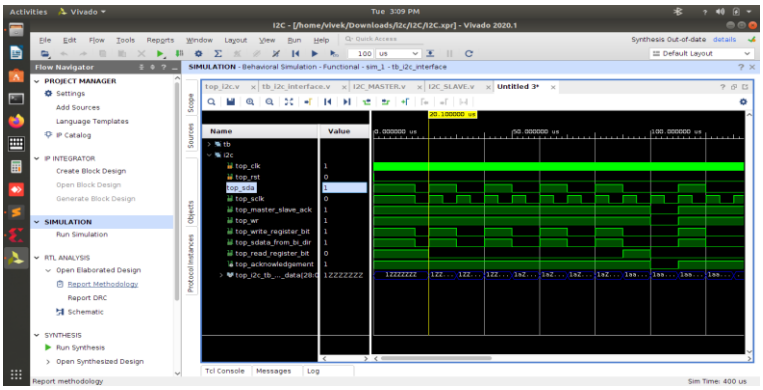

Fig. 1 Simulation Results

In the fig 2, it shows the Synthesis Results of the corresponding I2C communication protocol.

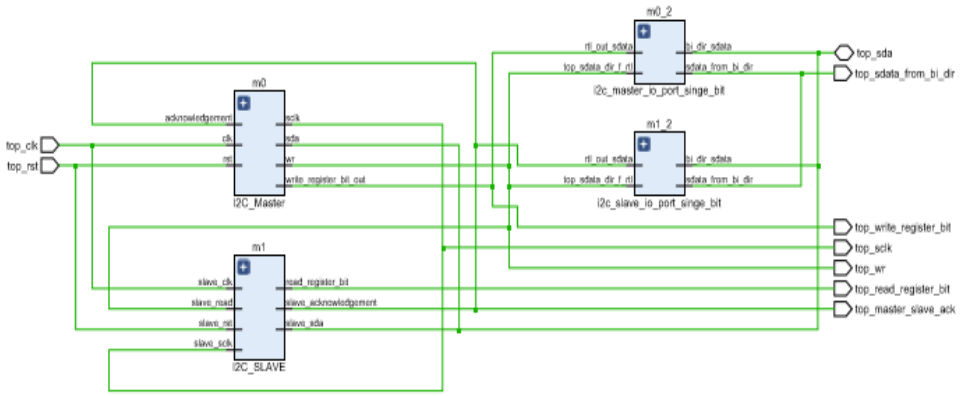

Fig. 2 Synthesis Results

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In Fig 3, it shows the Design Summary of the corresponding I2C communication protocol.

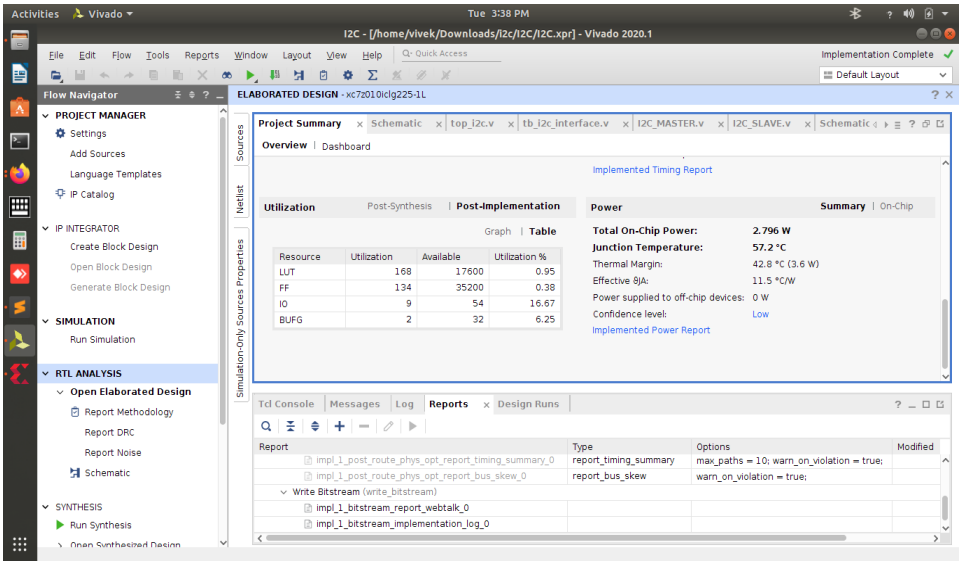

Fig .3 Design Summary

In Fig 4, it shows the Power Summary of the corresponding I2C communication protocol

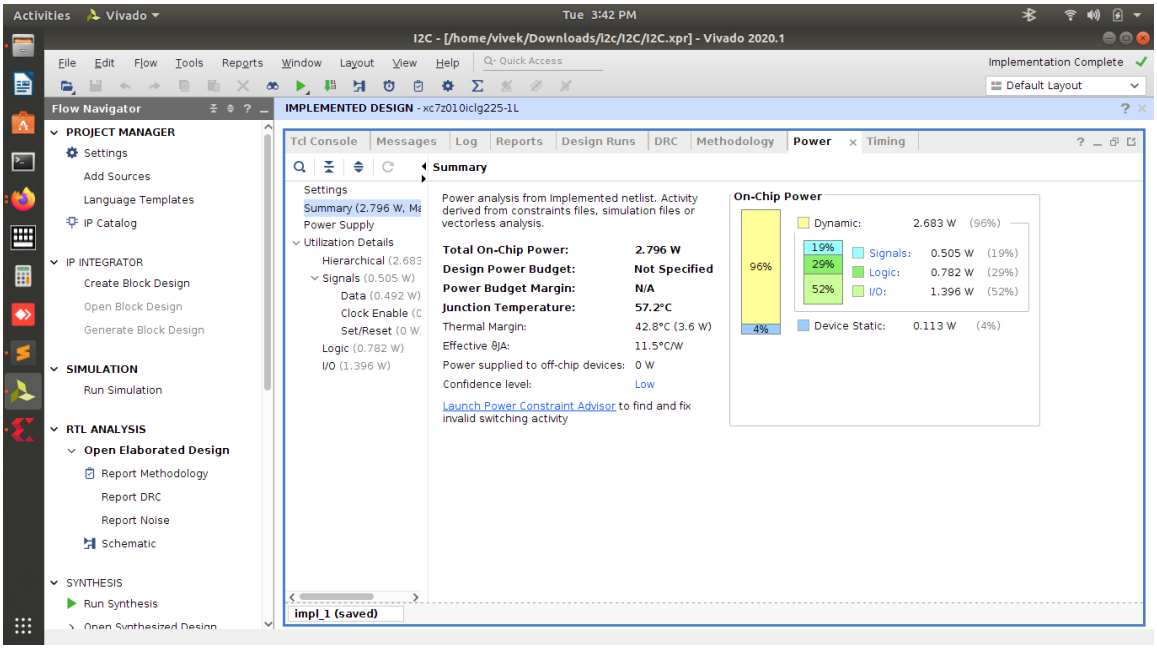

Fig .4 Power Summary

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VI.CONCLUSION

An I2C is the easy and cheap communication protocol, it can be multi-master or multi-slave. In I2C we get the acknowledgment (ACK) and not acknowledgment (NACK) bits after the each transmitted byte. I2C is an industry standard protocol which is used in many applications such as accessing EEPROM or accessing Real Time Clock. Some disadvantage also attaches with I2C, it is a half-duplex communication and slow as compared to SPI (serial peripheral communication) and it can cover shorter distance. I2C bus is used by many integrated circuits and is simple to implement. Any microcontroller can communicate with I2C devices even if it has no special I2C interface. I2C specifications are flexible – I2C bus can communicate with slow devices and can also use high speed modes to transfer large amounts of data. Because of many advantages, I2C bus will remain as one of the most popular serial interfaces to connect integrated circuits on the board.

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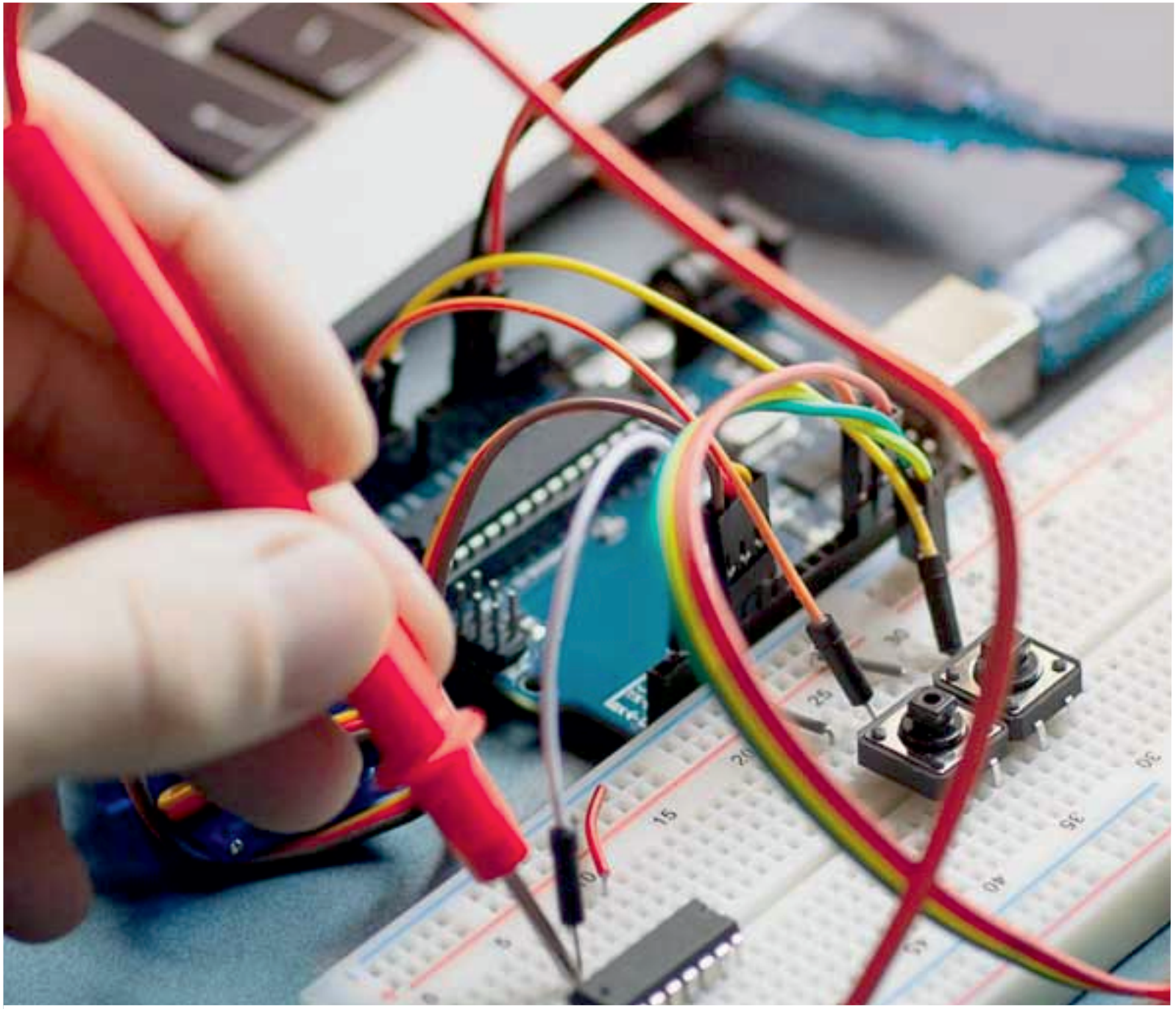

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